PARALLEL PROCESSING APPLICATION TO NON-LINEAR MICROWAVE NETWORK DESIGN

M. I. Sobhy and Y. A. R. El-Sawy

Electronic Engineering Laboratories,
The University of Kent at Canterbury,
Canterbury, Kent, CT2 7NT,
U.K.

ABSTRACT

One of the objectives of this paper is to introduce microwave network designers to an important new development in computer-aided design techniques. The paper describes how parallel processing is applied to the CAD of non-linear microwave circuits. The advantage of parallel processing is the significant reduction in computational time such that optimisation becomes feasible even on a desk-top computer. The developed programs run on an AT desk-top with a transputer board capable of concurrent processing speeds of over 40 MIPS. A new representation of microwave and non-linear circuits has been developed to suit the required parallelism. Applications to the analysis of non-linear amplifiers, frequency multipliers and microwave mixers are described.

I. INTRODUCTION

There are a number of available computer programs for analysing linear and non-linear microwave networks (2-4). Both time-domain and harmonic balance methods are based on serial processing. They both require powerful computers and no optimisation is offered due to the inordinate time required. In order to reduce the computational time and hardware requirements, a new approach for the circuit simulation is required. This paper describes such an approach which is suitable for parallel processing. The process does not require iteration when solving the non-linear network. Furthermore, each circuit element has an identifiable process and all the processes work in parallel. These properties result in a very efficient algorithm that can be mounted on a desk-top AT computer with a transputer board. The algorithm also offers the possibility of optimisation due to the improvement in computational speed and the fact that each element is assigned an identifiable process.

II. OUTLINE OF THE METHOD

Any CAD procedure has to satisfy both Kirchoff's law and the I-V relations of the elements (linear, non-linear, integral, differential, delay .., etc.). Instead of representing the network by using circuit diagrams, the new theoretical development derives a signal flow or simulation diagram for each network and can be summarised, in a simple form, as follows:

After defining a network tree, Kirchoff's laws are expressed in the hybrid form

$$\begin{bmatrix} i_t \\ \hline v_c \end{bmatrix} = \left[\begin{array}{c|c} 0 & D \\ \hline -D^T & 0 \end{array}\right] \begin{bmatrix} v_t \\ \hline i_c \end{bmatrix} \qquad (1)$$

where the subscripts t and c refer to the tree and cotree elements respectively and the matrix D is the dynamical transports matrix (1). Equation (1) is a hybrid form of Kirchoff's laws with some elements represented by Kirchoff's first law and some by the second law.

The I-V relations are given by

$$\begin{aligned} i_t &= f_1(v_t) \\ v_c &= f_2(i_t) \end{aligned} \qquad (2)$$

where f_1 and f_2 are general functions that could be non-linear and/or differential.

Figure (1) shows a block simulation diagram of the circuit which is a representation of equations (1) and (2). This process is very general and can be applied to any linear or non-linear network.

The advantage of this formulation is that each element in the circuit is considered a "process" and all processes together with Kirchoff's first and second laws operate in 'parallel'. This is certainly not the case when trying to solve a circuit from its circuit diagram as all the I-V relations in the circuit are interdependent and it is very difficult to define any parallelism.

The advantages are summarized as follows:-

1. Either a parallel or a sequential algorithm can be written to analyse the system.
2. No iterations are required to obtain the solution.
3. Each element has a clearly defined process.

CH2725-0/89/0000-0645$01.00 © 1989 IEEE

Thus varying the element values to optimise the network response is easily achieved without reformulating the equations.

4. There are no restrictions on either the topology or the type of processes. Each process can be a linear, non-linear or any desired function.

5. The overall system can be easily configured on a number of transputers.

III. BASIC PROCESS

A library of processes had to be developed to simulate all the possible circuit elements together with basic signal manipulative processes such as addition, subtraction, fan-out, .. etc.

1. Lumped and non-linear elements: All linear and non-linear elements can be represented as shown in Figure 2a. The inputs to the process are currents and voltages on the element itself (designated as the input i) or on any other signal in the network (designated as control c). The output o is given by the function f(i,c). This function can be either a simple multiplication (for resistors or conductors), integration or differentiation (for capacitors and inductors) or any other linear or non-linear function. Thus modelling any active or passive device is achieved by determining the input i, control c and the function f(i,c).

2. Distributed elements: Although distributed elements can also be represented by the general process shown in Figure 2a, it is useful to give more details of the process involved. An example is given in Figure 2b which is a process representing a lossless transmission line. The inputs to the process are the input and output voltages V_1 and V_2 of the transmission line and the outputs from the process are the currents I_1 and I_2. Other combinations are also possible.

3. Signal manipulation process: The three signal manipulation processes are shown in Figures 2(c-f). These are the signal addition (or subtraction), the delta (or fan-out) process and a delay process.

4. Probe process: For interactive testing of the circuit, the user may wish to attach a 'probe' to any point in the circuit to inspect the signal at that point.

IV. HARDWARE

The program has been implemented on a desk-top AT computer with the addition of five Transputers. The 'Transputer' is a trademark of INMOS Ltd. and is a processor which implements the process model of communication embodied in its native parallel programming language 'OCCAM'. Each transputer has four hardware links, each of which can be mapped to a bi-directional pair of OCCAM channels. Any number of transputers can be used, however, the systems of five transputers were found adequate for good programming efficiency. One of the five transputers was used as a 'Host' to act as an interface between the user and the remaining four transputers network which carries out the execution of the algorithm. The Host transputer has 1 Mbyte of dedicated DRAM and each of the other four transputers has 256 kbytes of dedicated DRAM. Theoretically, the computation time is inversely proportional to the number of transputers used. In practice, the efficiency of configuring the network and the finite communication time between transputers will affect the reduction in time.

V. APPLICATIONS

The developed program has been applied to several microwave networks.

The following summarises some of the results obtained.

1. Non-linear amplifier: The amplifier circuit shown in Figure 3a was analysed. The initial result from the program is the waveform in the time-domain as shown in Figure 3b. The results could be analysed further to obtain the saturation characteristics and the frequency response as shown in Figures 3c and 3d.

2. Frequency doubler: The MESFET 4-8GHz frequency doubler circuit shown in Figure 4a was analysed from 0-800 ps at 1 ps intervals and took 130 seconds of computer time. Further analysis of the results gives a 5.5dB conversion gain for the doubler. The waveform and the frequency response are shown in Figures 4b and 4c respectively.

3. Mixers and oscillators: Mixer and oscillator circuits have also been analysed and the results will be presented at the symposium.

VI. CONCLUSIONS

A new, powerful algorithm has been developed for analysing non-linear microwave networks using parallel processors. The system offers the possibility of analysing and optimising these circuits using low-cost desk top computers and eliminates the need for workstations or mainframes. By identifying every circuit element with a process, efficient optimisation is feasible. Further increase in speed is possible by the simple addition of more transputers without any further modification of the software.

REFERENCES

(1) M. I. Sobhy and M. H. Keriakos, "Computer aided analysis and design of networks containing commensurate and non-commensurate delay lines", IEEE Trans. MTT-28 No. 4, pp. 348-358, April, 1980.

(2) V. Rizzoli et al, "User oriented software package for the analysis and optimisation of non-linear microwave circuits". IEE Proc. Part H, Vol.33, Oct. 1986, pp. 635-640.

(3) M. I. Sobhy and A. K. Jastrzebski, "Computer-aided design of microwave integrated circuits", Proc. 14th European Microwave Conference, pp. 705-710, Liege, 1984.

(4) M. I. Sobhy and A. K. Jastrzebski, "Direct integration methods of non-linear microwave circuits", 15th European Microwave Conference, pp. 1110-1118, Paris, Sept. 1985.

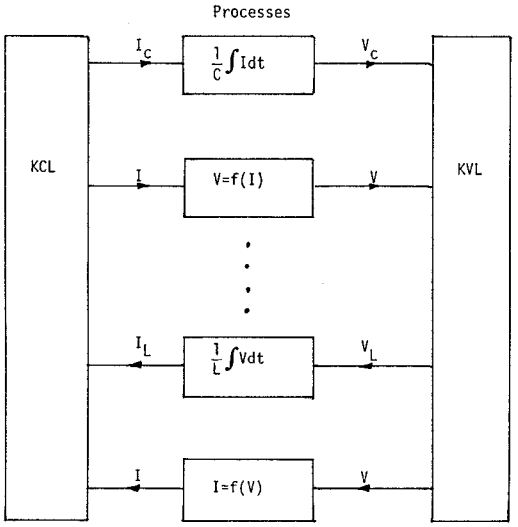
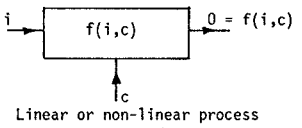
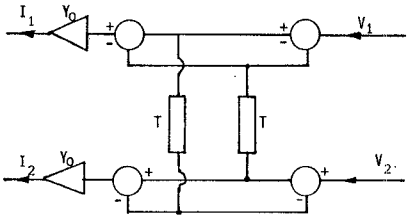


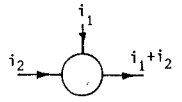
Figure 1: Scheme for Parallel Processing



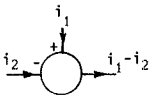
(a) Linear or non-linear process



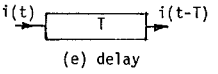
(b) Distributed elements



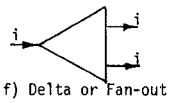
(c) Signal addition



(d) Subtraction

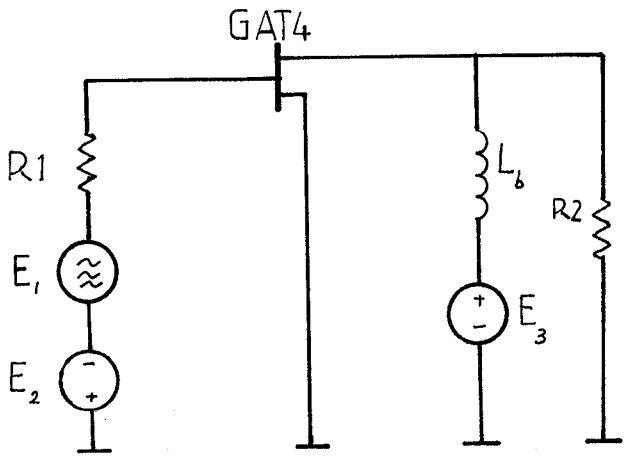


(e) delay

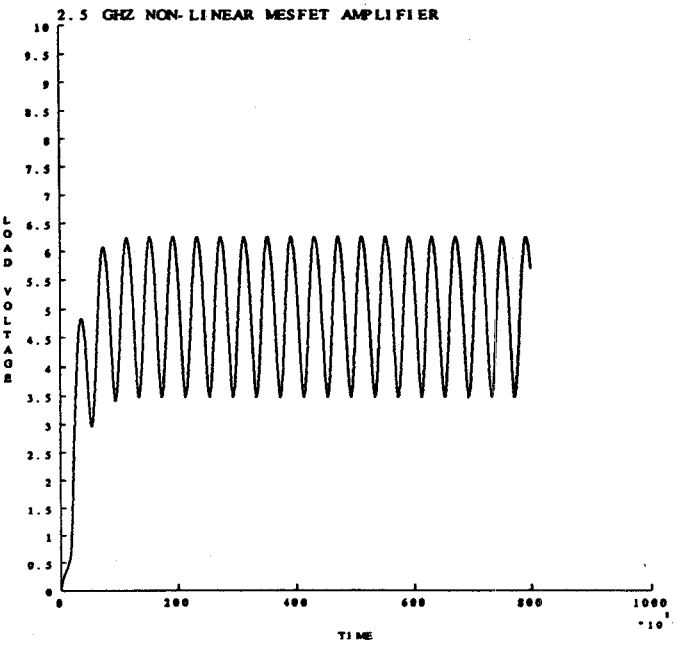


(f) Delta or Fan-out

Figure 2: Basic Processes



3 (a) Non-linear amplifier



(b) Response in time domain

Fig.3b: Non-linear microwave amplifier and response from transputer.

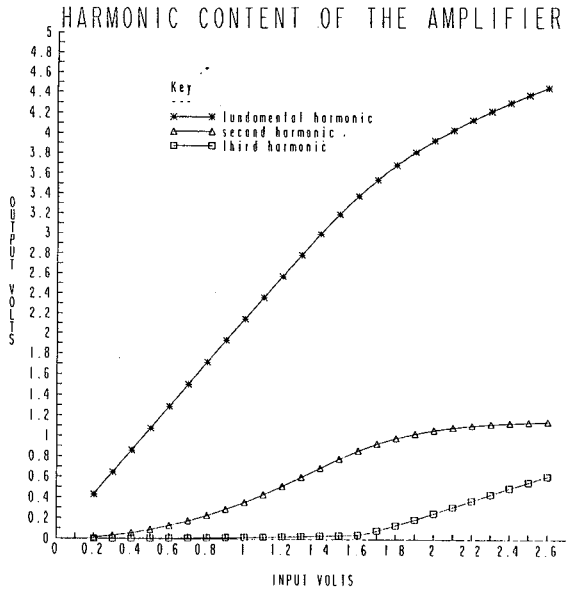


Figure 3(c): Saturated characteristics of amplifier

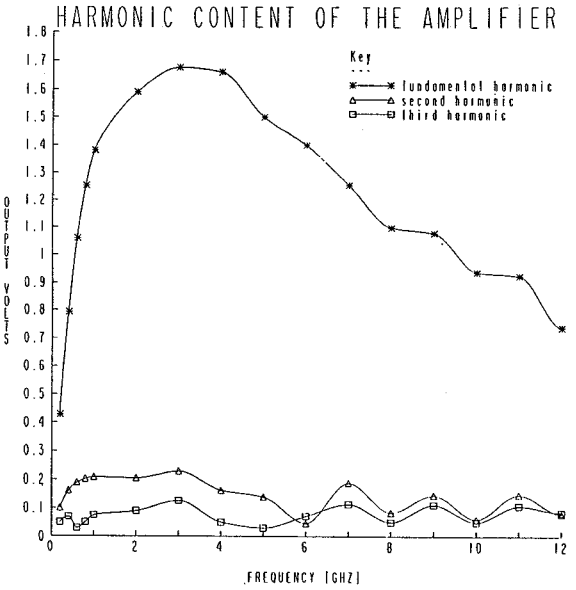


Figure 3(d): Large signal frequency response of amplifier

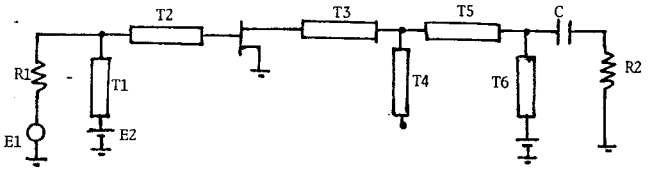


Fig. 4(a): Circuit diagram of 4-8 GHz doubler

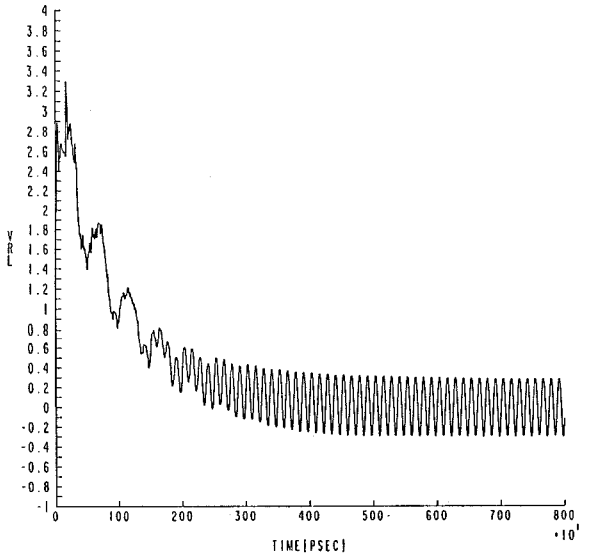


Figure 4(b): Output of 4-8 GHz Doubler

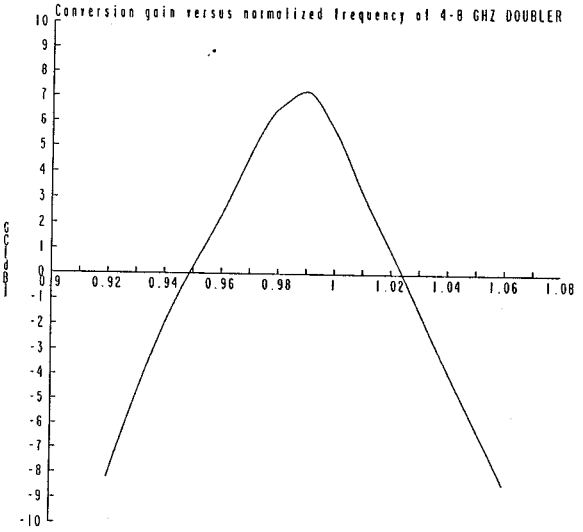


Figure 4(c): Frequency response of 4-8 GHz Doubler